A High-Power-Handling GSM Switch IC with New Adaptive-Control-Voltage-Generator Circuit Scheme

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Abstract — **We propose a high-power-handling switch circuit using a new adaptive-control-voltage-generator circuit (AVG). This AVG enables the internal control node voltages to be automatically increased in high-input-power conditions. This switch circuit results in high-power-handling, low-insertion-loss, small chip size and low voltage control. The developed IC demonstrated a handling power of 36.5 dBm and an insertion loss of 0.31 dB with 40% chip size reduction.**

I. INTRODUCTION

The use of wireless communication systems, such as digital cellular-phones and wireless LANs, has been increasing worldwide at a brisk pace. A development of multi-mode/band terminals, for example digital cellular-phone combined with wireless LAN, will be increasing from now on. In these multi-mode/band terminals, composites of functions and/or miniaturization without any degradation of performances are required for components using in those terminals.

An antenna switch is one of the key RF components for wireless communication terminals. Conventionally low-cost and high-power-handling Si p-i-n diode switches have widely been used for GSM application. However, as a switch function is more complicated, e.g. mPnT for multi-mode/band terminals like GSM/WCDMA, a GaAs-FET based switch IC becomes advantageous in order to reduce current consumption and/or chip size at lower control voltages.

We proposed and demonstrated a low-insertion-loss and high-handling-power switch circuit [1]. However, that circuit still has an issue on miniaturization for complicated switching function. In most conventional circuits, decrease in chip size leads to decreasing handling power and/or increasing insertion loss. This is because a conventional circuit [1]-[3] usually has a stacked FET configuration and wide gate width to achieve both high handling power and low insertion loss.

This paper describes a proposal of a switch circuit using a new adaptive control voltage generator with high-power-handling and low-insertion-loss as well as small chip size and discusses the measured results of switch IC adopting this new circuit.

II. CIRCUIT DESIGN

A. Trade-off between handling power and insertion loss

Figure 1 shows a conventional single-pole dual-throw (SPDT) switch. This switch has two switch blocks, Tx and Rx, that have stacked FETs and resistors (Rg). This stacked configuration is needed to achieve high-power handling capability. The maximum handling power of an antenna switch (Pmax) is given by [1]-[5];

$$P_{\max} = \frac{2[n(V_{RF} + Vt)]^2}{Z_0} \quad , \qquad (1)$$

where n is the stacked number of FETs, Vt is the threshold voltage of FET, Z_0 is the system impedance, and V_{RF} is the DC voltage of RF terminals. This equation indicates that V_{RF} must be increased as n decreases in order to maintain the handling power.

However, an additional problem is encountered in increasing V_{RF} to reduce the FET stack-number because there is large insertion loss. Insertion loss depends on the on-state resistance (R_{on}) and the off-state capacitance (C_{off}). In the range of the control voltage used in our experiments, C_{off} was hardly changed, thus, leading us to assume that C_{off} is constant. Hence, insertion loss can only be

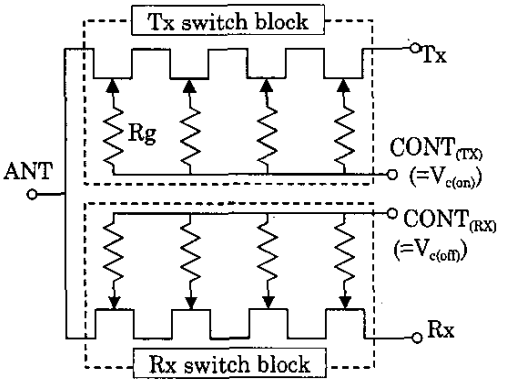

Figure 1. Schematic of conventional SPDT switch circuit

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determined by using R_{on}, which is given by;

$$R_{on} \propto \frac{n}{W_g\left(V_{C(on)} - V_{RF} - V_t\right)} \quad , \qquad (2)$$

where Wg is the gate width of FET and the $V_{C(on)}$ is control voltage for on state FETs. Thus, increasing V_{RF} in order to decrease the FET stack-number leads to large insertion loss.

Figure 2 shows Pmax as a function of V_{RF} at a Vt of -0.5 V. When the control voltage is +3.0/0 V, V_{RF} settles at a voltage of about 2.7 V. Therefore, it needs 5 stacked FETs to exceed 36 dBm for GSM applications in a conventional circuit. In order to decrease the FET stacked number to 4 with a handling power of 36 dBm, V_{RF} needs to be increased over 3.0 V.

This is fundamental issue of a conventional antenna switch circuit. A new circuit that can solve this issue is described in the next section.

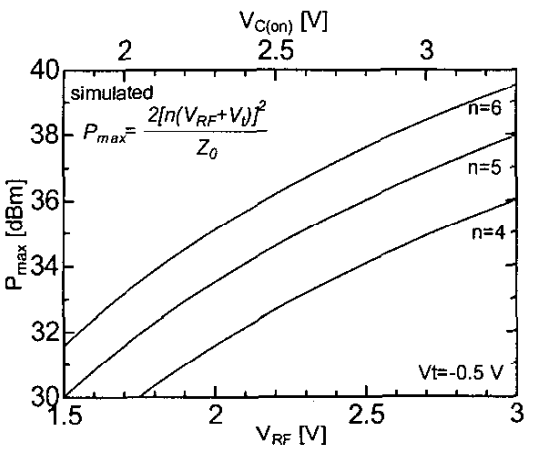


Figure 2. Power capability characteristics

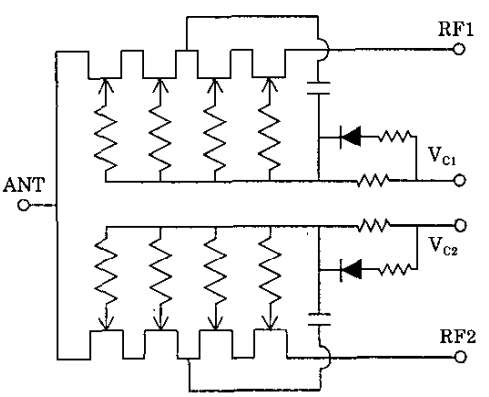


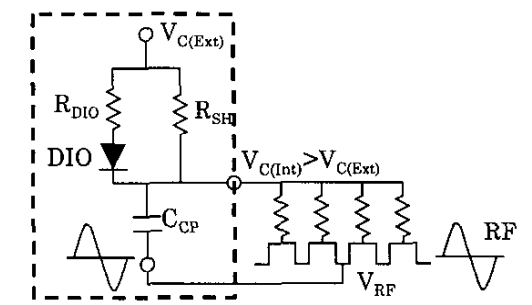
Figure 3. Schematic of new SPDT switch circuit

B. A switch circuit with new adaptive-control-voltage-generator circuit scheme

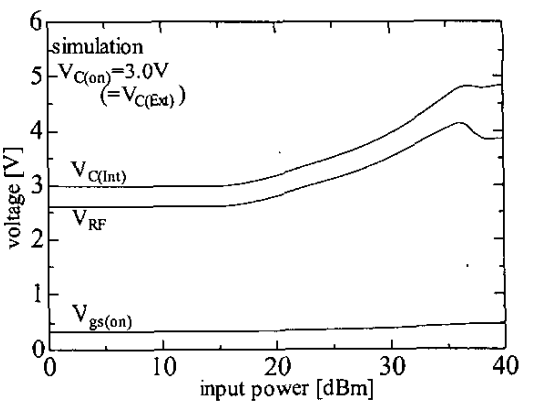
Figure 3 shows the new SPDT antenna switch. This circuit configuration has an adaptive-control-voltage-generator (AVG). Figure 4(a) shows the circuit configuration of the AVG. This AVG contains a capacitor for detecting RF signals, a diode as charge transfer device and two resistors for diode current suppression and a shunt. Since the diode current increases as RF signal power increases, the output voltage of AVG ($V_{C(Int)}$) increases. Therefore, this circuit acts as charge pump and generates a higher voltage than $V_{C(Ext)}$ in high input power conditions. Figure 4(b) shows a simulation result for DC voltage by connecting an AVG with SPDT switch circuit, which is shown in Fig. 3. Figure 4(b) shows that the internal control voltage increases as RF signal power increases. On the other hand, $V_{gs(on)}$ is hardly changed when internal control voltage increases, where $V_{gs(on)}$ is given by

$$V_{gs(on)}=V_{C(Int)}-V_{RF} \qquad . (3)$$

Consequently, since the AVG can generate a higher



(a) Circuit diagram



(b) DC bias

Figure 4. Switch IC with a adaptive-control-voltage-generator (AVG)

control voltage than $V_{C(on)}$ while maintaining $V_{gs(on)}$, the new switch circuit can provide high handling power with low insertion loss when the FET stack number decreases. In other words, when the chip size is constant, this circuit can decrease control voltage while maintaining high RF performance. Thus, the issues described in the previous section can be overcome without any degradation in performance.

III. Device Fabrication and Performances

Developed SPDT switch ICs were fabricated using the GaAs heterojunction FET (HJFET) process [6]. An InGaAs channel, which has double-doped electron-supplying layers, was used to reduce R_{on}.

A microphotograph of the developed SPDT switch IC is shown in Fig. 5. The SPDT uses 4-stacked FETs, and the chip area is 975×880 um, which is 40% smaller than conventional SPDT switch IC using 5-stacked FETs.

Figure 6 compares the power transfer characteristics between the novel circuit and conventional circuit at control voltages of +3.0/0 V and +2.0/0 V. The novel circuit exhibited a handling power of 36.5 dBm at a control voltage of +3.0/0 V. This circuit can also improve power-handling characteristics at low voltages.

Figure 7 shows the characteristics of the 2nd and 3rd-order harmonics at a control voltage of +3.0/0 V. The harmonic characteristics are clearly correlated to handling power. Thus, the harmonics of this circuit are also improved compared to the conventional circuit. The 2nd and 3rd-order harmonics are −69 dBc and −78 dBc, respectively, at an input power of 35 dBm.

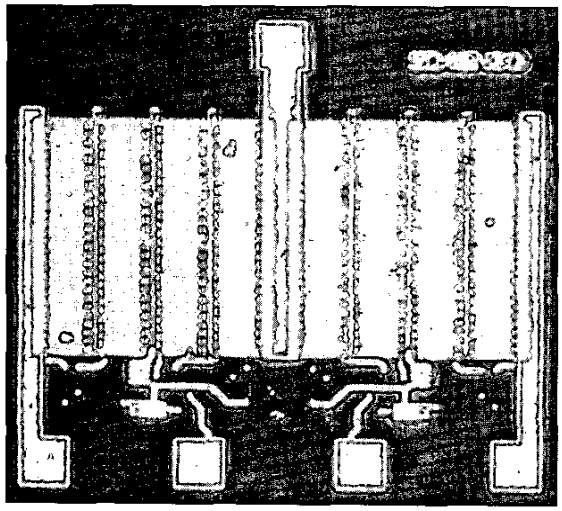


Figure 5. Chip microphotograph

The frequency responses of this circuit and a conventional circuit at the control voltage of +3.0/0 V and +2.0/0 V are shown in Fig. 8. The insertion loss of this circuit is 0.31 dB and the isolation is −22.4 dB at 1 GHz.

Figure 9 shows a comparison of the normalized handling power and insertion loss [1]-[4]. The normalized data is given by $P_{-0.1dB}/(n^2 V_{RF}^2)$. This figure shows that our circuit can produce a very high handling-power capability while being small in size. The performance of the fabricated IC is summarized in Table I. Measured V_{RF} is also summarized in Table I. Table I shows that V_{RF} increases when input signal power increases. Through the design optimization of AVG, V_{RF} can settles at a much higher voltage so that handling power is increased to be suitable for GSM applications in a much smaller chip size and at a much lower control voltage.

IV. Conclusion

A GaAs SPDT switch IC using a new circuit configuration was developed. This circuit configuration using adaptive-control-voltage-generator (AVG) results in high-handling-power, low-insertion-loss, small chip size and low-control-voltage.

The switch IC we developed using AVG demonstrated a handling power of 36.5 dBm and an insertion loss of 0.31 dB with a control voltage of +3.0/0 V with 40% smaller chip size. This circuit also performed well at a control voltage of +2.0/0 V.

Moreover, by design optimization of AVG, handling power is increased in a much smaller chip and at a much lower control voltage.

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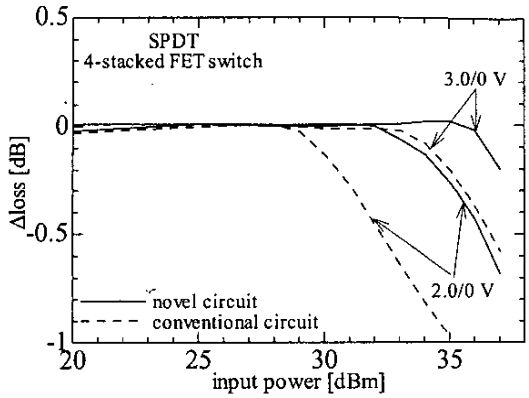

Figure 6. Input power dependence

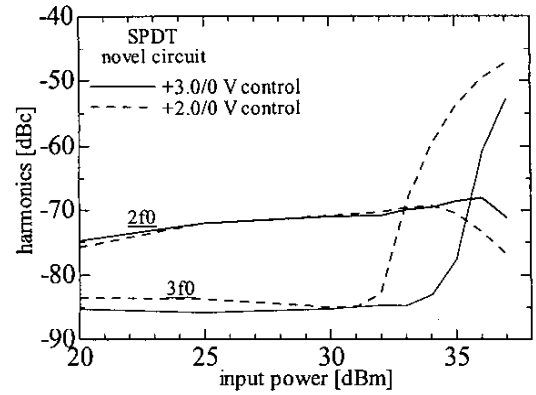

Figure 7. Input power dependence of harmonics

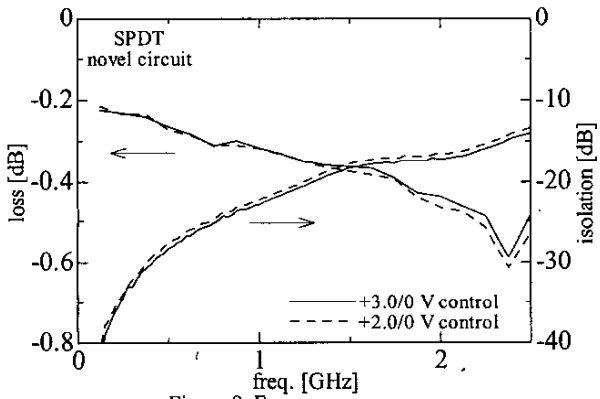

Figure 8. Frequency response (insertion loss and isolation)

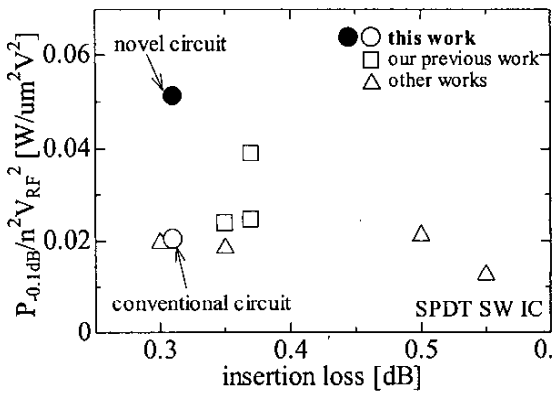

Figure 9. Comparison between normalized handling power potential of conventional and developed SPDT switch ICs

TABLE I

CHARACTERISTICS OF FABRICATED SPDT SWITCH ICS

novel circuit	insertion loss		isolation		$P_{-0.1dB}$	Harmonics		V_{RF}	
	1 GHz	2 GHz	1 GHz	2 GHz		2f0	3f0	0 dBm	30 dBm
+3.0/0 V control	0.31 dB	0.44 dB	-22.4 dB	-16.7 dB	36.5 dBm	-69 dBc (@35 dBm)	-78 dBc (@35 dBm)	2.67 V	3.98 V
+2.0/0 V control	0.31 dB	0.47 dB	-22.3 dB	-16.6 dB	34 dBm	-69 dBc (@33 dBm)	-68 dBc (@33 dBm)	1.75 V	2.53 V